White Paper

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Emerging Rugged Small Form Factor Mezzanine Technology

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1 INTRODUCTION

Modern aerospace and defense platforms require higher processing capability, greater I/O density, and improved signal integrity while simultaneously shrinking in size and operating within tighter thermal envelopes. As mission systems evolve to support advanced sensors, AI workloads, and distributed architectures, designers are increasingly constrained by SWaP demands and the limitations of legacy mezzanine standards. Against this backdrop, the recent introduction of the VITA 93 QMC specification presents new opportunities for embedded system designers and rugged integration labs that require high-speed, high-density I/O within harsh environments. QMC enables a significantly smaller mezzanine footprint compared to PMC, XMC, or VPX while preserving the rugged mechanical and environmental characteristics.

2 OVERVIEW OF VITA 93 QMC

QMC is designed for both performance and flexibility in that it supports high-speed serial data links through its defined Carrier interface, along with its user defined I/O interface. QMC was designed specifically to support a range of carrier card formats with varied deployed environments and supporting both Air and Conduction Cooled designs.

Being part of the VITA ecosystem allows existing standards like PMC, XMC, and VPX to benefit from QMC qualities.

Main technical highlights:

- Rugged, small form factor
- Modular, scalable
- High speed connectors with a defined pinout

2.1 Mechanical Features

2.1.1 Board Size

Typical mezzanines like PMC or XMC measure 149mm in length by 74mm in width, which can take up valuable real estate in a system. This is where QMC shines. A single width QMC mezzanine measures just 78.25mm in length and 26mm in width. This provides a balance between board layout and space constraints.

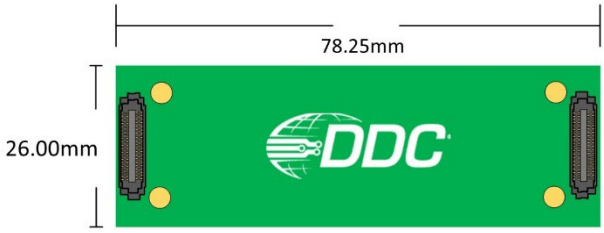

Figure 1. VITA 93 QMC Mezzanine

2.1.2 Connector choice

The connectors chosen for VITA 93 were carefully selected with high density I/O requirements and high speed signaling in mind. QMC mezzanines will utilize Samtec's AcceleRate® HD Ultra-Dense, Slim Body Arrays.

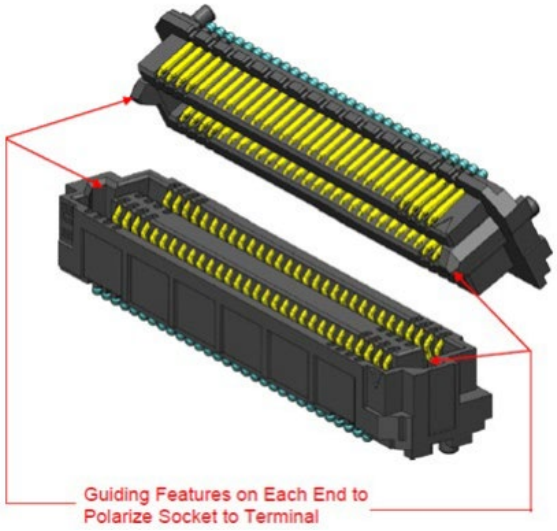

Figure 2. Samtec ASP-239729-x

The connectors are capable of PCI-e Gen 6 speeds, and are able to provide the user various densities of I/O pins depending on the width of the QMC. The environmental qualifications of the connectors are based on various EIA-364 testing.

QMC carrier designers will be able to implement varying height mating connectors to accommodate mezzanines with differing component heights.

QMC Module Connector	QMC Carrier Connector Heights	BO Parameter	Stacking Height "QMC_STACK"
7.5 mm QMC Module Connector	1.5 mm	0.1 mm	9.1 mm
7.5 mm QMC Module Connector	3.5 mm	0.1 mm	11.1 mm
7.5 mm QMC Module Connector	6.5 mm	0.1 mm	14.1 mm
7.5 mm QMC Module Connector	8.5 mm	0.1 mm	16.1 mm

Figure 3. QMC Mezzanine/Carrier Stacking Heights

2.1.3 Cooling Schemes

Just like other mezzanine standards, such as XMC, VPX, etc., QMC will also employ the cooling methods that are prevalent in the industry, which are Air Cooled and Conduction Cooled. Historically, other mezzanine designers could struggle with designing a product that could be both Air Cooled and Conduction Cooled often leading to multiple product designs. The QMC specification is defining that a single QMC design can be Air Cooled or upgraded to Conduction Cooled within the same design.

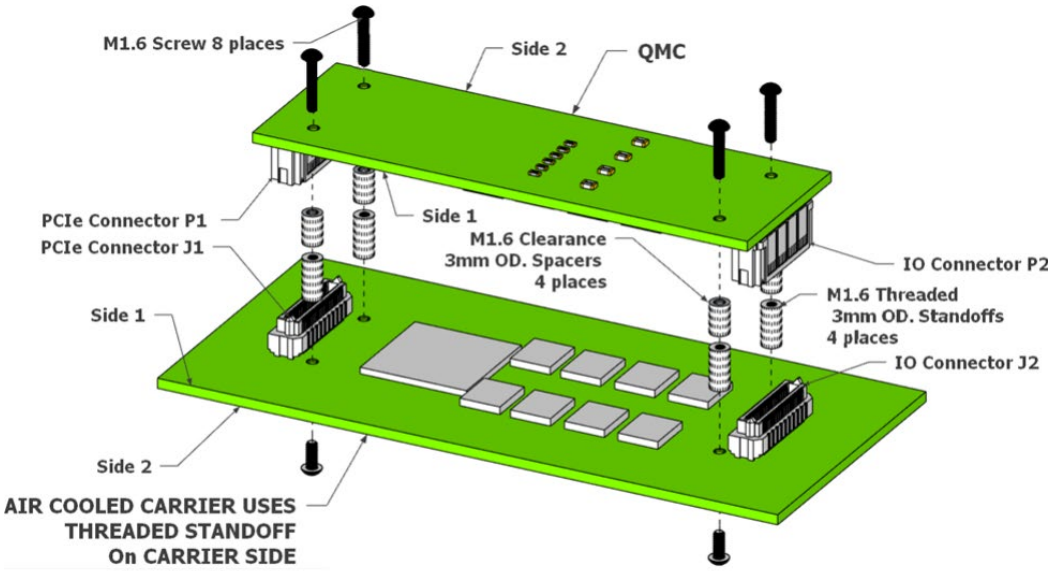

Figure 4. Air Cooled QMC

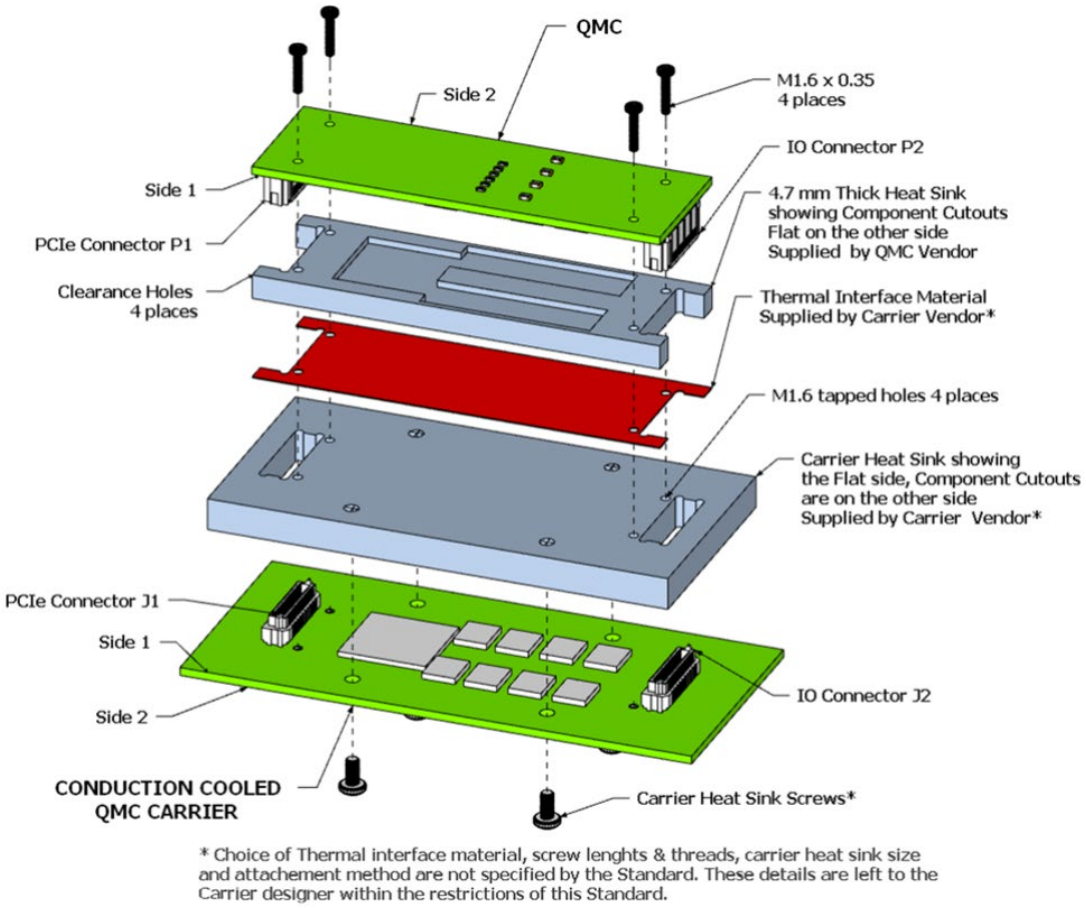

Figure *5*. Conduction Cooled QMC

2.2 Scalability

One of QMC's strongest quality is the ability to scale the design upwards to provide more I/O and provide more PCI-e bandwidth while maintaining the SWaP characteristics.

A mezzanine can be scaled from a single width QMC to a double, triple or quad QMC. A single width mezzanine offers PCI Express x4 lanes and 40 I/O pins. The I/O pins and PCI-e lanes are increased as a mezzanine is scaled up.

- **Double-wide**
  - PCIe x8
  - 80 I/O
- **Triple-wide**
  - PCIe x12
  - 120 I/O
- **Quad-wide**
  - PCIe x16
  - 160 I/O

A quad-wide QMC contains more I/O signals than a VITA 42/VITA 61 XMC.

QMC gives Data Device Corporation's (DDC) wide range of I/O and protocols, that are currently supported today, a large blank canvas to work with. Because QMC can accommodate signals that are low-speed and/or high-speed in nature, protocols like MIL-STD-1553, ARINC 429 or Ethernet and Time Sensitive Networking, can be designed into QMC mezzanines to leverage these scalability features.

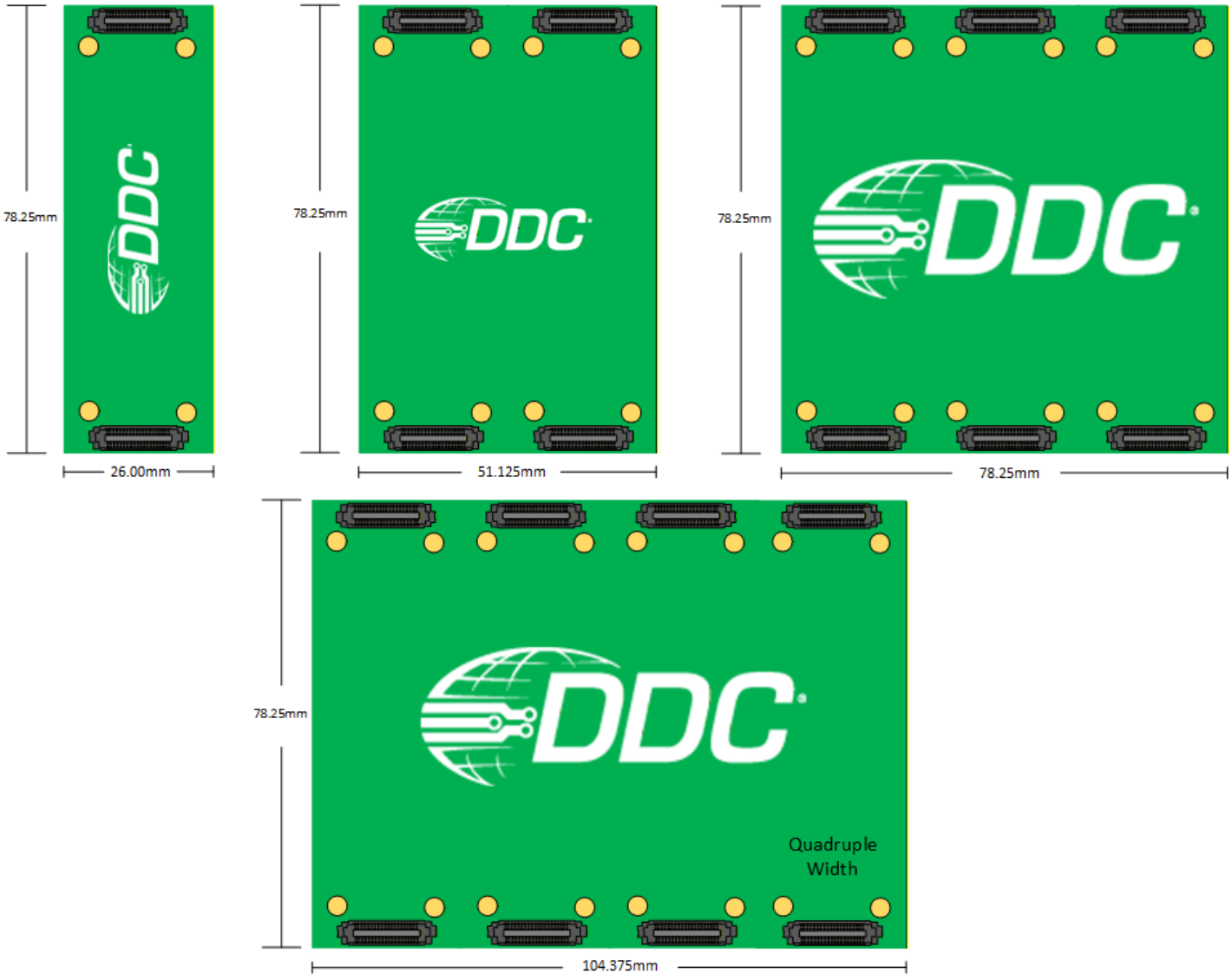

Figure 6. Scalable options

2.3 Electrical Interfaces

Existing mezzanine technology like PMC, XMC, and VPX offer various pin groups and layouts, which eventually lead the industry to create standards, such as SOSA, to limit variations and define a set group of pins.

QMC looks to build upon that and provide a user a defined pinout on both the Host interface and User I/O interface. This alleviates the worry of having to support differing pin groups.

2.3.1 Host Interface

One of the connectors on the QMC mezzanine handles the interface to the host system. The pinout contains the signals for voltage, PCI-e signals, JTAG, I^2C and management interfaces like IPMI. This is similar in ways to a P15 connector on an XMC card.

The QMC mezzanine is specified to draw certain amounts of current on each of the different voltage rails. The QMC mezzanine shall draw no more than 1.8A per host connector on the 12V rail, no more than 2.4A per host connector on the 3.3V rail, and maximum current draw of 10mA per host connector on the 3.3V AUX rail.

The QMC standard allows for different PCI Express Bifurcations so a user can benefit from the ability to scale the PCI-e lanes.

Table 5.8-1: Example of PCI Express Bifurcation

Counts of PCIe Lanes	# of x16	1												
	# of x12		1	1	1	1	1	1						
	# of x8								2	1	1			
	# of x4		1			1				2	2	4		
	# of x2			1			1						4	
	# of x1				1			1						4
QMC Site 4	PCIe Lane 15	x16	x4	NU	NU	x12	x12	x12	x8	x4	x8	x4	NU	NU
	PCIe Lane 14													
	PCIe Lane 13			x2									x2	
	PCIe Lane 12				x1									x1
QMC Site 3	PCIe Lane 11		x12	x12	x12					x4		x4	NU	NU
	PCIe Lane 10													
	PCIe Lane 9												x2	
	PCIe Lane 8													x1
QMC Site 2	PCIe Lane 7								x8	x8	x4	x4	NU	NU
	PCIe Lane 6													
	PCIe Lane 5												x2	
	PCIe Lane 4													x1
QMC Site 1	PCIe Lane 3					x4	NU	NU			x4	x4	NU	NU
	PCIe Lane 2													
	PCIe Lane 1						x2						x2	
	PCIe Lane 0							x1						x1

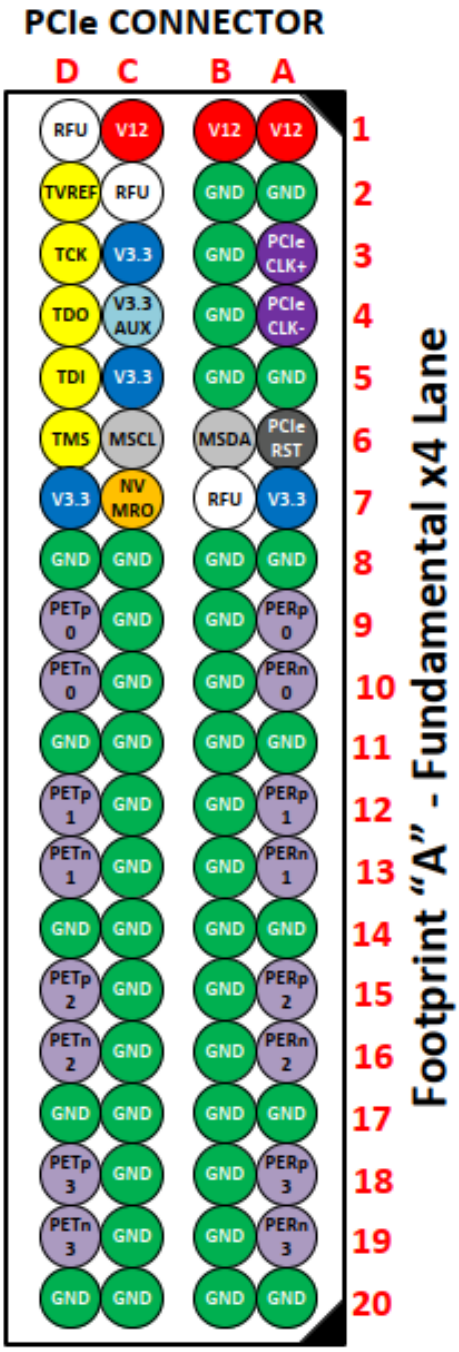

Figure 7. PCI-e Connector & Bifurcations

2.3.2 User I/O Interface

The User I/O connector also has a defined pinout as opposed to the various pin groups (X8d, X12d, etc.) found on a P16 connector for XMC mezzanines.

The user I/O pins are organized into five IOPIPEs each offering 8 single-ended / 4 differential signals. This design supports interfaces that require isolation.

Each type of signal requires specific routing impedances. Signals shall have an impedance of 40-60 Ohm for single-ended and 100 Ohm +/-10% for differential.

As mentioned previously, the scalability of QMC allows for more I/O signals than a traditional PMC/XMC. Each user I/O connector on a QMC follows the same pinout but can provide different I/O. For instance, on a quad-width QMC module, a user can have 160 I/O signals at their disposal.

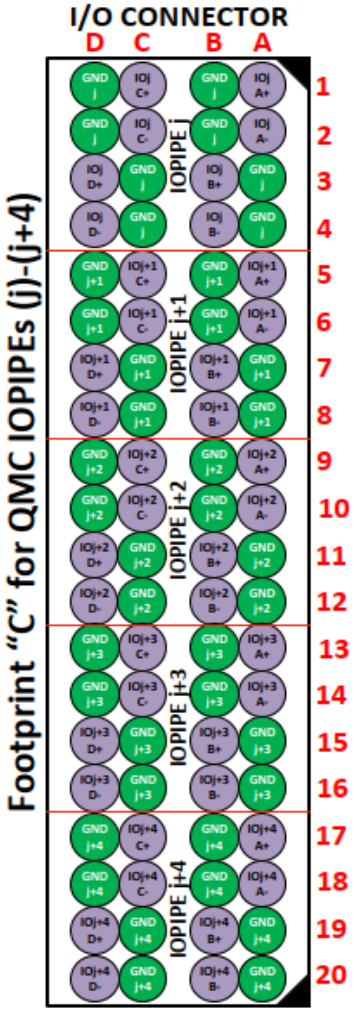

Figure 8. User I/O Pinout

3 SUMMARY/CONCLUSION

QMC's inherent rugged qualities combined with the defined pinout and scalability, provides system designers with a powerful new form factor that can address many needs within the aerospace and defense markets. Data Device Corporation (DDC) is looking to leverage this technology to enhance our industry leading portfolio of rugged embedded and test products.